IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	
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Celaya, Phillip C. et al	:	Group Art Unit: 3742
	:	
Serial No.: 09/817,330	:	
	:	
Filed: March 26, 2001	:	Examiner: Thiem D. Phan

For: METHOD OF MAKING A LEAD-FREE INTEGRATED CIRCUIT PACKAGE

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FAX No. (703) 872-9306 on April 26, 2004

By Signature: Lydia McNamara

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13 PAGES TOTAL

APPEAL BRIEF

I. REAL PARTY OF INTEREST

The real party of interest in this appeal is Semiconductor Components Industries, LLC (SCI), doing business as ON Semiconductor.

II. RELATED APPEALS AND INTERFERENCES

Applicants are not aware of any related appeals or interferences to this application.

III. STATUS OF THE CLAIMS

Claims 19-37 remain in the application and are the claims on appeal. A copy of the claims is provided in Appendix A.

Claims 1-18 have been cancelled in view of a restriction requirement.

IV. STATUS OF THE AMENDMENTS

A response to the Final Rejection was filed and the proposed amendment will be entered upon filing this appeal.

IV. SUMMARY OF THE INVENTION

The present invention relates to a method for making semiconductor devices with plated conductive structures. As described in the Background of the Invention on page 1, lines 25-36, semiconductor ball grid array (BGA) packages suffer from a high manufacturing cost because complex equipment is needed to pick up and place small solder balls onto access pads located on BGA substrates. This manufacturing process requires that the access pads be sufficiently large enough to account for solder ball movement during subsequent reflow processes, which increases package sizing and decreases packing density. Additionally, BGA solder balls contain lead, which is considered to be an environmental and health hazard.

As described on page 5, lines 21-33, the method of the present invention comprises plating a conductive material onto exposed access pads to form a lead-free lead that

projects outwardly from an integrated circuit package. In one embodiment, a photoresist layer is patterned with openings over the access pads to provide a mask for forming the lead-free leads.

As stated on page 7, lines 6-23, the leads are formed with a plating process to improve their flexibility and better control their height, which results in a higher reliability. In addition, the invention eliminates the need for lead-based or other types of solder balls to form the leads, thereby reducing the cost of the package and the risk of health or environmental damage. Moreover, because a masking layer is used, smaller access pads may be used, which provides for smaller packages and higher packing density.

VI. ISSUE

Whether claims 19-37 are patentable under 35 U.S.C. §102(a) over Jin-Sung Kim (USP 6,162,664).

VII. GROUPING OF THE CLAIMS

Claims 19, 20, 31, and 32-35 stand or fall together.
Claims 21 and 28 stand or fall together.
Claim 22 stands or falls alone.
Claims 23-27 stand or fall together.
Claim 29 stands or falls alone.
Claim 30 stands or falls alone.
Claims 36-37 stand or fall together.

VIII. ARGUMENT

The Examiner has rejected claims 19-37 under 35 U.S.C. 102(a) as being anticipated by Kim ('664).

Claims 19, 20, 31, 32, and 33-35 stand or fall together. Independent claim 19 calls for a method of making an integrated circuit, comprising the step of plating a conductive material to project outwardly from a second surface of a substrate to form a lead-free lead of the integrated circuit. Similarly, independent claim 32 calls for, among other things, plating a conductive material to extend outwardly from a second surface of a substrate to form a lead-free lead of an integrated circuit.

The Examiner states that '664 teaches a method of making a semiconductor chip package comprising the steps of providing a substrate for mounting a semiconductor die and plating a lead (Pb)-free conductive material made of Ni-Au to project the lead (Pb)-free first lead of copper and Ni-Au outwardly from the substrate.

Applicants acknowledge that '664 discloses an alternative to lead (Pb) for metal plating layer 60, which is only one layer of multiple layers of the lead shown by '664. However, '664 shows leads 30 (or double layer bumps) further comprised of a flat base layer 40 (copper), a metal plating layer 60 (Ni-Au or Sn-Pb), and a solder layer 50 (Sn-Pb) (see col. 4, lines 13-37 and FIG. 5 of '664), not just metal plating layer 60. Thus, none of the leads 30 of '664 are lead (Pb)-free as applicants claim.

More specifically, '664 teaches that metal plating layer 60, which can be comprised of either a Ni-Au or a Sn-Pb, is part of base layer 40. Solder layer 50, which is only described as being comprised of tin (Sn) and lead (Pb), is formed by screen printing onto base layer 40 (see col. 4, lines 33-36 of '664). Each lead 30 is comprised of this

combination of layers, thus '664 only teaches to form leads comprised of or with lead (Pb).

Thus, because applicants claim at least one lead (Pb)-free lead, not just one of the layers of the lead to be lead (Pb)-free as '664 teaches, '664 cannot anticipate claims 19 and 32.

Claims 20 and 31 depend from claim 19 and are believed allowable over the '664 reference for at least the same reasons as claim 19.

Claims 33-35 depend from claim 32 and are believed allowable over the '664 reference for at least the same reasons as claim 32.

Claims 21 and 28 stand or fall together. Claim 21 depends from claim 19 and further calls for a step of forming a signal path on the first surface with the conductive material. Claim 21 is believed allowable for the same reasons as claim 19. Additionally, applicants assert that claim 21 is allowable over the '664 reference because the '664 reference does not show a method of forming a signal path with the same conductive material used to form a lead-free lead as required by claim 21.

Claim 28 depends from claim 21 and is believed allowable for at least the same reasons as claim 21.

Claim 22 stands or falls alone. Claim 22 depends from claim 21 and further calls for disposing the conductive material in a via defined by the substrate to extend the signal path from the first surface to the second surface of the substrate. Claim 22 is believed allowable for the same reasons as claims 19 and 21. Additionally, applicants assert that claim 22 is allowable over the '664 reference because the '664 reference does not show a method of further disposing the conductive material in a via defined by the substrate to extend the signal path from the first surface to the second surface of substrate as required by claim 22.

Claims 23-27 stand or fall together. Claim 23 depends from claim 22 and further calls for disposing the conductive material on the second surface to extend the signal path from the via to the lead-free first lead. Claim 23 is believed allowable for the same reasons as claims 19 and 22. Additionally, applicants respectfully submit that claim 23 is allowable over the '664 reference because the '664 reference does not show a method of further disposing the conductive material on the second surface to extend the signal path from the via to the lead-free first lead as required by claim 23.

Claims 24-27 depend from the claim 23 and are believed allowable for at least the same reasons as claim 23.

Claim 29 stands or falls alone. Claim 29 depends from claim 19 and further includes a step of forming a solder mask on the second surface between the lead-free first lead a lead-free second lead of the integrated circuit. Claim 29 is believed allowable for the same reasons as claim 19. Also, applicants respectfully submit that claim 29 is allowable over the '664 reference because the '664 reference does not show a forming a second lead-free lead or forming a solder mask between the first and second lead-free leads as is called for in claim 29.

Claim 30 stands or falls alone. Claim 30 depends from claim 29 and further calls for forming the solder mask after the step of plating. Claim 30 is believed allowable for the same reasons as claim 29. Further, claim 30 is believed allowable over the '664 reference because the '664 reference fails to show forming a solder mask after a step of plating as required by claim 30.

Claims 36 and 37 stand or fall alone. Independent claim 36 calls for, among other things, disposing a conductive material along the first surface and through a via of the substrate to form a signal path of the integrated

circuit between the first and a second surface of the substrate, and plating the conductive material on the second surface to form a lead-free lead of the integrated circuit that is electrically coupled to the signal path. Applicants respectfully submit that claim 36 is allowable over the '664 reference because the '664 reference fails to show disposing a conductive material along a first surface and through a via in a substrate to form a signal path between first and second surfaces where the conductive material on the second surface forms a lead-free lead.

As stated above, '664 discloses an alternative to lead (Pb) for metal plating layer 60. However, '664 shows leads 30 comprised of a flat base layer 40 (copper), a metal plating layer 60 (Ni-Au or Sn-Pb), and a solder layer 50 (Sn-Pb) (see col. 4, lines 13-37 and FIG. 5 of '664). Thus, none of the leads 30 of '664 are lead (Pb)-free as applicants claim.

More specifically, '664 teaches that metal plating layer 60, which can be comprised of either a Ni-Au or a Sn-Pb, is part of base layer 40. Solder layer 50, which is only described as being comprised of tin (Sn) and lead (Pb), is formed by screen printing onto base layer 40 (see col. 4, lines 33-36 of '664). Each lead 30 is comprised of this combination of layers, thus '664 only teaches to form leads comprised of or with lead (Pb).

Thus, because applicants claim at least one lead (Pb)-free lead, not just one of the layers of the lead to be lead (Pb)-free as '664 teaches, '664 cannot anticipate claim 36.

Claim 37 depends from claim 36 and is believed allowable for at least the same reasons as claim 36.

In view of the above, it is believed that the claims are allowable, and the Board of Appeals and Interferences is respectfully requested to reverse the Examiner.

Respectfully submitted,

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APPENDIX A

Claims

19. (Previously Amended) A method of making an integrated circuit, comprising the step of plating a conductive material to project outwardly from a second surface of a substrate to form a lead-free first lead of the integrated circuit.

20. (Previously Amended) The method of claim 19, further comprising the step of mounting a semiconductor die to a first surface of the substrate.

21. (Previously Amended) The method of claim 20, further comprising the step of forming a signal path on the first surface with the conductive material.

22. (Previously Amended) The method of claim 21, further comprising the step of disposing the conductive material in a via defined by the substrate to extend the signal path from the first surface to the second surface of the substrate.

23. (Previously Amended) The method of claim 22, further comprising the step of disposing the conductive material on the second surface to extend the signal path from the via to the lead-free first lead.

24. (Previously Amended) The method of claim 23, wherein the step of disposing the conductive material on the second surface includes the step of forming an access pad on the second surface.

25. (Previously Amended) The method of claim 23, further comprising the steps of:

disposing a photoresist layer on the second surface;

patterning the photoresist layer to expose the access pads; and

plating the conductive material on the access pads.

26. (Original) The method of claim 25, wherein the step of patterning includes the step of forming an opening in the photoresist layer over the access pads.

27. (Original) The method of claim 26, wherein the step of plating includes the step of plating the conductive material within the opening.

28. (Previously Amended) The method of claim 21, further comprising the step of wire bonding the signal path to a node of the semiconductor die to couple a signal between the node and the lead-free first lead.

29. (Previously Amended) The method of step 19, further comprising the step of forming a solder mask on the second surface between the lead-free first lead and a lead-free second lead of the integrated circuit.

30. (Original) The method of claim 29, wherein the step of forming includes the step of forming the solder mask after the step of plating.

31. (Previously Amended) The method of claim 19, wherein the step of plating includes the step of plating the conductive material in an outward direction for routing a current (I_{SIGNAL}) through the lead-free first lead that flows parallel to the outward direction.

32. (Previously Amended) A method of forming an integrated circuit, comprising the steps of:

providing a substrate having a first surface for mounting a semiconductor die; and

plating a conductive material to extend outwardly from a second surface of the substrate to form a lead-free lead of the integrated circuit.

33. (Original) The method of claim 32, wherein the step of plating includes the step of disposing the conductive material to a height for attaching the lead to a mounting surface.

34. (Original) The method of claim 33, wherein the step of disposing includes the step of disposing the conductive material to the height of at least fifty micrometers.

35. (Original) The method of claim 33, wherein the step of disposing includes the step of forming the lead to a height that maintains a spacing between the substrate and the motherboard.

36. (Previously Amended) A method of making an integrated circuit, comprising the steps of:

mounting a semiconductor die to a first surface of a substrate;

disposing a conductive material along the first surface and through a via of the substrate to form a signal path of the integrated circuit between the first and a second surface of the substrate; and

plating the conductive material on the second surface to form a lead-free lead of the integrated circuit that is electrically coupled to the signal path.

37. (Previously Amended) The method of claim 36, wherein the step of plating includes the step of plating the conductive material to project outwardly from the second surface.